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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/724,618	12/02/2003	Motoi Ashida	67161-133	2587

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McDermott, Will & Emery  
600 13th Street, N.W.  
Washington, DC 20005-3096

EXAMINER
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QUACH, TUAN N

ART UNIT	PAPER NUMBER
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2826

DATE MAILED: 06/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/724,618

Applicant(s)

ASHIDA, MOTOI

Examiner

Tuan Quach

Art Unit

2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 15 April 2005.
- 2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-6 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-6 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01 December 0203 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

### DETAILED ACTION

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Young.

Regarding claim 1, Young (4,851,257) teaches a semiconductor device comprising a semiconductor substrate 10 having two types of active regions that are PMOS region and an NMOS region separated from each other in plan view by an PN separation film 20/420, a dual gate 72/212/451 extending linearly across the PMOS region, the PN separation film and the NMOS region collectively on an upper side of the semiconductor substrate 10/400, the dual gate electrode including a P type portion positioned on the PMOS region and an N type portion positioned on the NMOS region, and a PN junction, e.g., 90a80a;40; 213b; 452 positioned between the P type portion and the N type portion, the PN junction including a silicide region e.g., regions 74, 219, 480 been subjected to silicidation, the silicide region, e.g., 75/219, is apart from both the PMOS and NMOS region and formed within an area of the PN separation film. See Figs. 1d-1e; 2b-2c; 4c-4d, column 5 line 4 to column 6 line 4 to column 6 line 25, column 7 line 10 to column 8 line 23, column 9 line 50 to column 10 line 63.

Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Liaw.

Art Unit: 2826

Regarding claim 1, Liaw teaches a semiconductor device comprising a semiconductor substrate 10 having two types of active regions that are PMOS region and an NMOS region separated from each other in plan view by an PN separation film 12, a dual gate 30/32 extending linearly across the PMOS region, the PN separation film and the NMOS region collectively on an upper side of the semiconductor substrate 10, the dual gate electrode including a P type portion 32 positioned on the PMOS region and an N type portion 30 positioned on the NMOS region, and a PN junction positioned between the P type portion and the N type portion, the PN junction including a silicide region 62 having been subjected to silicidation, the silicide region 62 is apart from both the PMOS and NMOS region and formed within an area of the PN separation film, e.g., Fig. 15. See Figs. 3-15, column 3 line 1 to column 5 line 62.

Regarding claims 2 and 3, the provision of the dual gate being substantially covered with a silicidation prevention film including a silicon nitride 36 except for the silicide region is shown in Figs. 4-6, 11A, 11B and 15, column 3 line 35 et seq.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-6 rejected under 35 U.S.C. 103(a) as being unpatentable over Liaw taken with Goto.

Regarding claim 1, Liaw are applied above but do not explicitly recite the reasons for a small area of silicide. Goto further shows the silicide contacts 27 joining the silicide in a decreased area defined by structure 12, e.g., areas 26a, 26b. See the abstract, Figs. 4F-4I, column 4 line 35 to column 6 line 58, column 7 line 58-67. It would have been obvious to one skilled in the art to have selected the area of silicidation including selecting a small area as taught by Goto since such permits a decreasing silicide connecting area connecting between p type region and n type region in the dual gate structure as taught by Goto and permitting reducing distance between active regions and improving integration level.

Regarding claim 2, in addition to the reasons delineated above, Goto further shows the coverage of all area except for the area covered by structure 12 thereby permitting silicide connecting are formed. It would have been obvious to one skilled in the art to have covered all areas except for the area where the silicide connecting the p and n junction of the dual gate as evidenced by Goto. Regarding claim 3, the use of silicon nitride as the silicide preventing area is well known as obvious as evidenced by Liaw as delineated above.

Regarding claim 4, although Liaw does not show a contact to active region overlapping the dual gate in plain view, Goto teaches the formation of contact 30/33 to active regions overlapping the gate patterns without direct contact with each other as the gate patterns are covered with insulating layers 15/21. See Fig. 3F, 5D, column 7 line 14-41. It would have been obvious to one skilled in the art in practicing Liaw to have included contacts to active regions overlapping the dual gate since such is

conventional and obvious wherein margin of alignment can be enhanced as the contacts to active regions are permitted to be overlapping the gate pattern without direct contact thereto.

Regarding claim 5 concerning the contact being positioned as to avoid the silicide region on the pn junction, such selection would have been conventional obvious as evidenced by Liaw, Fig. 13 and 15, and by Goto as shown above and further do not require the contact being position to the silicide region on the pn junction, wherein such would avoid unwanted contact to the pn junction when the desired contact is to be made to the active regions.

Regarding claim 6, concerning the contact being positioned to avoid the PN separation in plain view, such selection would have been obvious as shown in Liaw and Goto as delineated above, wherein such contact is not required or desired to be made to such separation region, and wherein such would avoid unwanted contact to the PN separation and wherein such would permit the desired contact to the active regions to be made and to avoid the possibility of contact to the separation region.

Applicant's arguments filed April 15, 2005 have been fully considered but they are not persuasive.

Applicant argues that the dual gate of P portion on PMOS and N portion on NMOS is not shown. Nonetheless such dual gate of P and N doping for corresponding regions in the CMOS is employed through out in Young. See, e.g., Fig. 1D, 2B, Fig. 4D, and the corresponding description including, e.g., column 5 lines 29-65, including, e.g., column 5 lines 50-52, column 7 lines 15 to column 8 line 34. That such provision is

Art Unit: 2826

notoriously conventional in the dual gate is admitted by applicant, page 1 lines 11-16.

The dual gate structure employed by applicant corresponds to the dual gate employed in the prior art admitted by applicant and the dual gate employed by Young delineated above, including, e.g., Figs. 1D, 2A-2C, 4D.

Applicant further argues that Liaw does not disclose that the silicide layer is placed apart from the PMOS region and the NMOS region and that Liaw teaches silicide region extend beyond the area of the PN separation film. This nonetheless fails to consider that the silicide on the PN junction area met the limitation, namely, that silicide is apart from the PMOS and NMOS and does not preclude other silicide regions form elsewhere. In any event, that clearly corresponds to an option shown in Liaw, column 4 line 57-58 where silicide contacts are not required to be employed on source or drains. Additionally, the limitation regarding the silicide within the PN separating region is met as shown in the figures, e.g., 14 and 15, and as the language "within" in the claims neither preclude nor exclude any silicide outside the separating region, namely the silicide is not required to be confined solely to be within the separating region and encompass region within as well as without or outside; the silicide further would be clearly apart from the PMOS and NMOS active regions as shown otherwise shorting would occur. In any event, such confinement would have been apparent as shown in Fig. 15 region 62 in Liaw, and as shown in Young, Fig. 2C above.

Regarding Goto, this reference clearly shows the motivation for one skilled in the art to have selected the area of silicidation including selecting a small area as taught therein since such permits a decreasing silicide connecting area connecting between p

Art Unit: 2826

type region and n type region in the dual gate structure as taught by Goto and permitting reducing distance between active regions and improving integration level. Accordingly, it would have been obvious to one skilled in the art in practicing Liaw to have included contacts to active regions overlapping the dual gate since such is conventional and obvious wherein margin of alignment can be enhanced as the contacts to active regions are permitted to be overlapping the gate pattern without direct contact thereto. Furthermore, regarding claim 5 concerning the contact being positioned as to avoid the silicide region on the pn junction, such selection would have been conventional obvious as evidenced by Liaw, Fig. 13 and 15, and by Goto as shown above and further do not require the contact being position to the silicide region on the pn junction, wherein such would avoid unwanted contact to the pn junction when the desired contact is to be made to the active regions. Additionally, regarding claim 6, concerning the contact being positioned to avoid the PN separation in plain view, such selection would have been obvious as shown in Liaw and Goto as delineated above, wherein such contact is not required or desired to be made to such separation region, and wherein such would avoid unwanted contact to the PN separation and wherein such would permit the desired contact to the active regions to be made and to avoid the possibility of contact to the separation region.

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within



TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Tuan Quach whose telephone number is 571-272-1717. The examiner can normally be reached on M-F from 8:30 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Nathan Flynn, can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Tuan Quach  
Primary Examiner